This talk presents an overview of 3D IC research at the Georgia Tech Computer-Aided Design (GTCAD) laboratory. First, we present 3D-MAPS (3D Massively Parallel Processor with Stacked Memory) V1 processor, a logic+memory 2-tier 3D IC that features 64 general-purpose processor cores and SRAM. Second, we investigate the multi-physics (= thermo-electro-mechanical) reliability issues in through-silicon-via (TSV)-based 3D ICs and develop EDA solutions. Third, we investigate the design benefits and challenges for monolithic 3D ICs, considered by many as the future of 3D ICs, where the individual tiers are ‘grown’ on top of each other, instead of being ‘bonded.’ Lastly, we present various low power design methods developed based on 3D IC implementations of ultraSPARC T2 processor (open source commercial processor with 500 million transistor) and 28nm PDK.

Biography
Sung Kyu Lim received the B.S., M.S., and Ph.D. degrees from the Computer Science Department, UC Los Angeles, in 1994, 1997, and 2000, respectively. He joined the School of Electrical and Computer Engineering, Georgia Institute of Technology in 2001, where he is currently a full Professor. His research focus is on the architecture, design, test, and EDA solutions for 3D ICs. His research on 3D IC reliability is featured as a Research Highlight in the Communication of the ACM in 2013. Dr. Lim received the National Science Foundation Faculty Early Career Development (CAREER) Award in 2006. He received the Best Paper Award from SRC TECHCON’11, TECHCON’12, and ATS’12. His work is nominated for the Best Paper Award at ISPD’06, ICCAD’09, CICC’10, DAC’11, DAC’12, and ISLPED’12. He led the Cross Center Theme on 3D Integration for the Focus Center Research Program (FCRP) of Semiconductor Research Corporation (SRC) during 2010-12.
Design, Test, and EDA Research for 3D ICs at GTCAD Laboratory
Sung Kyu Lim, Professor
School of Electrical and Computer Engineering
Georgia Institute of Technology

Abstract
This talk presents an overview of 3D IC research at the Georgia Tech Computer-Aided Design (GTCAD) laboratory. First, we present 3D-MAPS (3D Massively Parallel Processor with Stacked Memory) V1 processor, a logic+memory 2-tier 3D IC that features 64 general-purpose processor cores and SRAM. This is arguably the first general-purpose many-core 3D processor ever developed in academia and fully tested using real applications. This 3D processor achieves up to 64GB/s memory bandwidth while consuming 4W power. This work is presented at the IEEE International Solid-State Circuits Conference (2012). We also present 3D-MAPS V2, a 5-tier extension of V1 that features 128 cores and 256MB wide-I/O 3D DRAM. We discuss the entire chip development spectrum (except manufacturing): architecture and verification, programming, design and sign-off analysis, package/board design, and testing. Moreover, we discuss our RTL-to-GDSII CAD tool flow that is based on various 2D IC commercial tools and our plug-ins to handle 3D ICs.

Second, we investigate the multi-physics (= thermo-electro-mechanical) reliability issues in through-silicon-via (TSV)-based 3D ICs and develop EDA solutions. We study how to model these complex phenomena, apply them to analyze the reliability of large-scale 3D circuits, and develop full-chip design methods to mitigate the issues. Third, we investigate the design benefits and challenges for monolithic 3D ICs, considered by many as the future of 3D ICs, where the individual tiers are “grown” on top of each other, instead of being “bonded”. The biggest benefit is the nano-scale inter-tier vias that are a few orders of magnitude smaller than TSVs. Monolithic 3D IC enables ultra-fine-grained 3D integration, which finds numerous applications in logic and memory systems. Lastly, we present various low power design methods developed based on 3D IC implementations of ultraSPARC T2 processor (open source commercial processor with 500-million transistor) and 28nm PDK.

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